UNIVERSITE M'HAMED BOUDHIAF M'SILA
FACULTE DE TECHNOLOGIE
DEPARTEMENT ELECTRONIQUE

MASTER 1 Instrumentation et Maintenance Industriel

M'SILA le 7/05/2017

Corrigé Examen d'Electronique Numérique Avancée : FPGA et VHDL

Exercice 1

```
-------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.all;
-------------------------------------
ENTITY dff IS
PORT (d, clk : IN STD_LOGIC;
q: OUT STD_LOGIC);
END dff;
-------------------------------------
ARCHITECTURE behavior OF dff IS
BEGIN
PROCESS (clk)
BEGIN
IF (clk'EVENT AND clk='1') THEN
q <= d;
END IF;
END PROCESS;
END behavior;
-------------------------------------
```

Exercice 2

```
-------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.all;
-------------------------------------
ENTITY dff IS
PORT (d, clk, rst: IN STD_LOGIC;
q: OUT STD_LOGIC);
END dff;
-------------------------------------
ARCHITECTURE behavior OF dff IS
BEGIN
PROCESS (clk, rst)
BEGIN
IF (rst='1') THEN
q <= '0';
ELSIF (clk'EVENT AND clk='1') THEN
q <= d;
END IF;
END PROCESS;
END behavior;
-------------------------------------
```

Exercice 3

```
-------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.all;
-------------------------------------
ENTITY dff IS
PORT (d, clk, rst: IN STD_LOGIC;
q: OUT STD_LOGIC);
END dff;
-------------------------------------
ARCHITECTURE behavior OF dff IS
BEGIN
PROCESS (clk)
BEGIN
IF (clk'EVENT AND clk='1') THEN
IF (rst='1') THEN
q <= '0';
else q <= d;
END IF;
END IF;
END PROCESS;
END behavior;
-------------------------------------------------------------------------
```

Exercice 4

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
       ENTITY compteur_decimal IS
                        PORT (
                                Clk, rst : IN STD_LOGIC;
                                cpt : OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
                                horloge_sortie : OUT STD_LOGIC
                              );
       END compteur_decimal;
-------------------------------------------------

        ARCHITECTURE rtl OF compteur_decimal IS
        SIGNAL s_cpt : STD_LOGIC_VECTOR(3 DOWNTO 0) := "0000";
          BEGIN
             PROCESS (clk, rst)
                BEGIN
                 IF rst = '1' then s_cpt <= "0000";

                    ELSIF clk'EVENT AND clk = '1' THEN
                          IF s_cpt >= 9 THEN
                                s_cpt <= "0000";
                          ELSE
                             s_cpt <= s_cpt + 1;
                          END IF;
                   END IF;
             END PROCESS;
      cpt <= s_cpt;
END rtl;
-------------------------------------------------------------------------
```